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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/685,877	10/11/2000	Yun-chan Myung	Q61029	3932

7590 12/18/2003

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EXAMINER	
SHAH, NILESH R	

ART UNIT	PAPER NUMBER
2127	6

DATE MAILED: 12/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No. 09/685,877	Applicant(s) MYUNG, YUN-CHAN	
	Examiner Nilesh R Shah	Art Unit 2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker et al (5,291,614) (hereinafter Baker)

As per claim 1, Baker teaches a real time control system of a multitasking digital signal processor, comprising: a ready queue including a ready queue link, the ready queue link comprising a first information indicating a first task control block for a sequentially first task among tasks in the digital signal processor, and a second task control block for a sequentially last task among the tasks in the digital signal processor (col. 4 lines 5-51, col. 10 line 10-65) ('For all three paths, the first steps 340, 348, and 352 are to save the contents of the DSP registers by storing the contents thereof in the task control block of the task being interrupted.') ('Referring now to the drawings, and first to FIG. 1, there is shown an exemplary data processing system comprising a personal computer 10 operable under an operating system to execute application programs'),

a priority link group of priority links, a number of the priority links being equal to a number of priority levels of the tasks in the digital signal processor (col. 12 lines 16- 59) ('Frame counter 452 includes a COUNT field that is decremented in response to each tick of clock 334. When the count reaches zero, step 454 then places task 2 in execution queue 358 in accordance with the priority of the task relative to other real-time tasks in the queue. Queue 358 includes both real-time and non-real-time tasks, the latter being executed when there are no real-time tasks remaining in the queue'), and

a second information indicating a third task control block for a sequentially first task among tasks having same priority among the tasks in the digital signal processor, and a fourth task control block for a sequentially last task among the tasks having same priority (col. 4 lines 5-51, col. 10 line 10-65, col. 12 lines 33-68, Fig 8) ('Referring now to the drawings, and first to FIG. 1, there is shown an exemplary data processing system comprising a personal computer 10 operable under an operating system to execute application programs ') ('Executor 332 then transfers control along one of three different paths dependent upon how it was invoked. For all three paths, the first steps 340, 348, and 352 are to save the contents of the DSP registers by storing the contents thereof in the task control block of the task being interrupted.') ('Each task has a Task Control Block (TCB) stored at a predetermined location in data store 104. The TCB provides system information about the task and a limited number of user links to other tasks' TCBs.');

and an operating system for setting the first and second information according to conditions of tasks for the digital signal processor, and controlling switching between the tasks of the ready queue (col. 4 lines 5-51, col. 10 line 10-65, col. 12 lines 33-68, Fig 8) ('FIG. 1, there is shown an exemplary data processing system comprising a personal computer 10 operable under an operating system to execute application programs ') ('Executor 332 then transfers control along one of three different paths dependent upon how it was invoked. For all three paths, the first steps 340, 348, and 352 are to save the contents of the DSP registers by storing the contents thereof in the task control block of the task being interrupted.'). Baker does not teach the use of transferring tasks over a network.

It is well know in the art of task management to transfer tasks over a network. It should be noted that what is claimed and what is disclosed in Baker differs only in the sense that in the claimed invention, tasks are being transferred over a network, while in Baker functions are transmitted over a network. In either case, data is being transferred over a communications system, and the form or function of that data is immaterial to what the scope of the invention is. Therefore, it would have been obvious to one of ordinary skill in the art to substitute the method of transmitting functions from a TCB as in Baker for tasks or any other type of data that is to be transmitted over a communications network. The discrepancy in type of data is immaterial, and the scopes of the inventions are essentially equivalent.

As per claim 2 Baker teaches a real time control system wherein the first information comprises a first list pointer corresponding to the first task control block and a second pointer

corresponding to the second task control block (col. 4 lines 5-51, col. 10 line 10-65) ('Referring now to the drawings, and first to FIG. 1, there is shown an exemplary data processing system comprising a personal computer 10 operable under an operating system to execute application programs ') ('The system also includes a scheduling clock 334 which operates at 9.6 Khz and generates on every clock "tick" an interrupt signal that invokes the foreground executor. The executor is also invoked in response to I/O transmit and receive commands 336, and read and write commands 338. Executor 332 then transfers control along one of three different paths dependent upon how it was invoked. For all three paths, the first steps 340, 348, and 352 are to save the contents of the DSP registers by storing the contents thereof in the task control block of the task being interrupted.'), and

the second information comprises a third list pointer corresponding to the third task control block and a fourth pointer corresponding to the fourth task control block (col. 4 lines 5-51, col. 10 line 10-65, col. 12 lines 33-68, Fig 8) ('Referring now to the drawings, and first to FIG. 1, there is shown an exemplary data processing system comprising a personal computer 10 operable under an operating system to execute application programs ') ('Executor 332 then transfers control along one of three different paths dependent upon how it was invoked. For all three paths, the first steps 340, 348, and 352 are to save the contents of the DSP registers by storing the contents thereof in the task control block of the task being interrupted.') ('Each task has a Task Control Block (TCB) stored at a predetermined location in data store 104. The TCB provides system information about the task and a limited number of user links to other tasks' TCBs.')

It is noted again that Baker teaches of a method for transmitting functions. As discussed for claim 1, the transfer of functions and records or any other type of data is analogous in the art of multicomputer data transferring, and is thus considered an insignificant difference.

As per claim 3 Baker teaches a real time control system wherein the operating system updates the first and second information so that deterministic scheduling with respect to the ready queue link and the priority link is maintained, when a task for the digital single processor is inserted or deleted (col. 10 line 10 –col. 11 line 32) ('The execution queue always has the task with the smallest COUNT at the top of the queue and those tasks with successively larger COUNTs toward the bottom of the queue. The task to be inserted is placed into the execution queue based on its updated COUNT value in comparison to the COUNT of the other tasks already in the queue. In case the inserted task has the same COUNT as a task which is already in the queue, it will get inserted after it. Thus, tasks which have the same COUNT will be executed by executor 356 in the same order in which they are linked to TMS.')

It is noted again that Baker teaches of a method for transmitting functions. As discussed for claim 1, the transfer of functions and records or any other type of data is analogous in the art of multicomputer data transferring, and is thus considered an insignificant difference.

As per claim 4, Baker teaches a real time control system further comprising a waiting queue including a waiting queue link, the waiting queue link comprising a third information indicating a fifth task control block for the sequentially first task among the tasks in the digital signal processor, and a sixth task control block for the sequentially last task among the tasks in the

digital signal processor (col. 10 line 10 –col. 11 line 32) ('The execution queue always has the task with the smallest COUNT at the top of the queue and those tasks with successively larger COUNTs toward the bottom of the queue. The task to be inserted is placed into the execution queue based on its updated COUNT value in comparison to the COUNT of the other tasks already in the queue. In case the inserted task has the same COUNT as a task which is already in the queue, it will get inserted after it. Thus, tasks which have the same COUNT will be executed by executor 356 in the same order in which they are linked to TMS.') ('Referring now to the drawings, and first to FIG. 1, there is shown an exemplary data processing system comprising a personal computer 10 operable under an operating system to execute application programs ') ('Executor 332 then transfers control along one of three different paths dependent upon how it was invoked. For all three paths, the first steps 340, 348, and 352 are to save the contents of the DSP registers by storing the contents thereof in the task control block of the task being interrupted.') ('Each task has a Task Control Block (TCB) stored at a predetermined location in data store 104. The TCB provides system information about the task and a limited number of user links to other tasks' TCBs.')

a second priority link group of second priority links, a number of the second priority links being equal to the number of priority levels of the tasks in the digital signal processor, and

a fourth information indicating a seventh task control block for the sequentially first task among the tasks having the same priority among the tasks in the digital signal processor, and an eighth task control block for the sequentially last task among the tasks having the same priority,

wherein the operating system sets the third and fourth information so that resources for the tasks of the waiting queue are deterministically acquired (col. 10 line 10 –col. 11 line 32) ('The execution queue always has the task with the smallest COUNT at the top of the queue and those tasks with successively larger COUNTs toward the bottom of the queue. The task to be inserted is placed into the execution queue based on its updated COUNT value in comparison to the COUNT of the other tasks already in the queue. In case the inserted task has the same COUNT as a task which is already in the queue, it will get inserted after it. Thus, tasks which have the same COUNT will be executed by executor 356 in the same order in which they are linked to TMS.') ('Referring now to the drawings, and first to FIG. 1, there is shown an exemplary data processing system comprising a personal computer 10 operable under an operating system to execute application programs ') ('Executor 332 then transfers control along one of three different paths dependent upon how it was invoked. For all three paths, the first steps 340, 348, and 352 are to save the contents of the DSP registers by storing the contents thereof in the task control block of the task being interrupted.') ('Each task has a Task Control Block (TCB) stored at a predetermined location in data store 104. The TCB provides system information about the task and a limited number of user links to other tasks' TCBs.')

It is noted again that Baker teaches of a method for transmitting functions. As discussed for claim 1, the transfer of functions and records or any other type of data is analogous in the art of multicomputer data transferring, and is thus considered an insignificant difference.

As per claim 5, Baker teaches a real time control system wherein the third information comprises a fifth list pointer corresponding to the fifth task control block and a sixth pointer corresponding

to the sixth task control block, and the fourth information comprises a seventh list pointer corresponding to the seventh task control block and an eighth pointer corresponding to the eighth task control block processor (col. 4 lines 5-51, col. 10 line 10-65, col. 12 lines 33-68, col. 13 lines 15-67, fig 8) ('Referring now to the drawings, and first to FIG. 1, there is shown an exemplary data processing system comprising a personal computer 10 operable under an operating system to execute application programs ') ('Executor 332 then transfers control along one of three different paths dependent upon how it was invoked. For all three paths, the first steps 340, 348, and 352 are to save the contents of the DSP registers by storing the contents thereof in the task control block of the task being interrupted.') ('Each task has a Task Control Block (TCB) stored at a predetermined location in data store 104. The TCB provides system information about the task and a limited number of user links to other tasks' TCBs.') ('SIA Pointer to task start instruction. RTOS passes control to the task at this location. If desired, the task can change this pointer to dynamically pass control to different sections of code within a task.')

It is noted again that Baker teaches of a method for transmitting functions. As discussed for claim 1, the transfer of functions and records or any other type of data is analogous in the art of multicomputer data transferring, and is thus considered an insignificant difference.

As per claim 6, Baker teaches a real time control system wherein the operating system controls the ready queue so that switching between the tasks is achieved on a basis of the priority link group, when task searching in the digital signal processor is based on an order of the priority of the tasks, (col. 10 line 10 –col. 11 line 32) (' Frame counter 452 includes a COUNT field that is

decremented in response to each tick of clock 334. When the count reaches zero, step 454 then places task 2 in execution queue 358 in accordance with the priority of the task relative to other real-time tasks in the queue. Queue 358 includes both real-time and non-real-time tasks, the latter being executed when there are no real-time tasks remaining in the queue. Tasks are dequeued and executed from the top of the queue and as each one is dequeued, the remaining real-time tasks are moved towards the top to await their turn. When task 2 reaches the top of the queue, and upon completion of the prior task or expiration of its allotted time, task 2 is then executed by transferring control by step 460 to the actual code 2 that performs the task. When task 2 completes execution, step 462 informs RTOS 300.')

and controls the ready queue so that switching between the tasks is achieved on a basis of the ready queue link, when the task searching is based on a first-in first-out (FIFO) system. (col. 10 line 10 –col. 11 line 32) ('The execution queue always has the task with the smallest COUNT at the top of the queue and those tasks with successively larger COUNTs toward the bottom of the queue. The task to be inserted is placed into the execution queue based on its updated COUNT value in comparison to the COUNT of the other tasks already in the queue. In case the inserted task has the same COUNT as a task which is already in the queue, it will get inserted after it. Thus, tasks which have the same COUNT will be executed by executor 356 in the same order in which they are linked to TMS.')

It is noted again that Baker teaches of a method for transmitting functions. As discussed for claim 1, the transfer of functions and records or any other type of data is analogous in the art of multicomputer data transferring, and is thus considered an insignificant difference.

As per claim 7, Baker teaches a real time control system further comprising a timer wheel for managing timer control blocks for the tasks in a pointer arrangement structure, wherein the operating system inserts the timer control blocks into corresponding slots of the timer wheel according to a time set for the tasks in the digital signal processor (col. 4 lines 5-51, col. 10 line 10-65, col. 12 lines 33-68, col. 13 lines 15-67, fig 8) ('Referring now to the drawings, and first to FIG. 1, there is shown an exemplary data processing system comprising a personal computer 10 operable under an operating system to execute application programs ') ('Executor 332 then transfers control along one of three different paths dependent upon how it was invoked. For all three paths, the first steps 340, 348, and 352 are to save the contents of the DSP registers by storing the contents thereof in the task control block of the task being interrupted.') ('Each task has a Task Control Block (TCB) stored at a predetermined location in data store 104. The TCB provides system information about the task and a limited number of user links to other tasks' TCBs.') ('SIA Pointer to task start instruction. RTOS passes control to the task at this location. If desired, the task can change this pointer to dynamically pass control to different sections of code within a task.')

It is noted again that Baker teaches of a method for transmitting functions. As discussed for claim 1, the transfer of functions and records or any other type of data is analogous in the art of multicomputer data transferring, and is thus considered an insignificant difference.

As per claim 8 baker teaches a real time control system wherein the timer wheel is divided into two timer wheels according to a predetermined reference time, and the operating system inserts timer control blocks corresponding to slots of the first timer wheel when the time set for the tasks

is equal to or less than the predetermined reference time, and inserts timer control blocks corresponding to slots of the second timer wheel when the time set for the tasks is greater than the predetermined reference time and equal to or less than twice the predetermined reference time (col. 4 lines 5-51, col. 10 line 10-65, col. 12 lines 33-68, col. 13 lines 15-67, fig 8) ('Referring now to the drawings, and first to FIG. 1, there is shown an exemplary data processing system comprising a personal computer 10 operable under an operating system to execute application programs ') ('The system also includes a scheduling clock 334 which operates at 9.6 Khz and generates on every clock "tick" an interrupt signal that invokes the foreground executor. The executor is also invoked in response to I/O transmit and receive commands 336, and read and write commands 338. Executor 332 then transfers control along one of three different paths dependent upon how it was invoked. For all three paths, the first steps 340, 348, and 352 are to save the contents of the DSP registers by storing the contents thereof in the task control block of the task being interrupted.') ('Each task has a Task Control Block (TCB) stored at a predetermined location in data store 104. The TCB provides system information about the task and a limited number of user links to other tasks' TCBs.') ('SIA Pointer to task start instruction. RTOS passes control to the task at this location. If desired, the task can change this pointer to dynamically pass control to different sections of code within a task.')

It is noted again that Baker teaches of a method for transmitting functions. As discussed for claim 1, the transfer of functions and records or any other type of data is analogous in the art of multicomputer data transferring, and is thus considered an insignificant difference.

As per claim 9, Barker teaches a real time control system wherein the operating system generates errors when the time set for the tasks is greater than twice the predetermined reference time (col. 4 lines 5-51, col.9 lines 1- 45, col. 10 line 10-65, col. 12 lines 33-68, col. 13 lines 15-67, fig 8) ('Referring now to the drawings, and first to FIG. 1, there is shown an exemplary data processing system comprising a personal computer 10 operable under an operating system to execute application programs ') ('Executor 332 then transfers control along one of three different paths dependent upon how it was invoked. For all three paths, the first steps 340, 348, and 352 are to save the contents of the DSP registers by storing the contents thereof in the task control block of the task being interrupted.') ('Each task has a Task Control Block (TCB) stored at a predetermined location in data store 104. The TCB provides system information about the task and a limited number of user links to other tasks' TCBs.') ('SIA Pointer to task start instruction. RTOS passes control to the task at this location. If desired, the task can change this pointer to dynamically pass control to different sections of code within a task.') ('step 268 then determines if the "wait count" has reached a preset value of seven to establish a maximum number eight of delayed cycles before the DSP will be halted. So long as the "wait count" is not seven, step 268 branches to step 270 which checks to see if the "DMA acknowledge" signal is active. If it is not, then a branch is made to step 272 which increments the wait count by one and branches back to step 268 to establish a loop that so long as the DMA acknowledge signal is inactive continues until the wait count equals seven and then a branch is made to step 274. Step 270 provides cycle timing for incrementing the wait count once each DSP cycle. During the course of a DSP cycle, which as previously indicated is divided into four phases, a determination is made e.g. in phase three as to whether the next cycle will involve the data

store. If the data store is not to be used on the next cycle, the DMA ACK signal is set active and control passes to 278 to complete the data transfer in the next cycle without halting the DSP')

It is noted again that Baker teaches of a method for transmitting functions. As discussed for claim 1, the transfer of functions and records or any other type of data is analogous in the art of multicomputer data transferring, and is thus considered an insignificant difference.

As per claim 10, Baker teaches a real time control system wherein a memory used to process the tasks in the digital signal processor is divided into an internal memory and an external memory in the digital signal processor, and the operating system manages the internal memory and the external memory using a memory structure made up of a start address, an end address, a memory size, a memory map, and next information indicating the start address of a next memory to be connected (col. 4 lines 5-63, col. 10 line 10-65)) ('BIC 16 performs two primary functions, one being that of a memory controller for accessing a main memory 30 and a ROM 32. Main memory is a dynamic random access memory (RAM) that comprises a plurality of single, in-line, memory modules (SIMMS) and stores application programs 31 for execution by microprocessor 12 and math coprocessor 18. ROM 32 stores a power on self test (POST) program 33. POST program 33 performs the primary test, i.e. POST, of the system when computer 10 is restarted by turning the power on or by a keyboard reset. An address and control bus 36 connects BIC 16 with memory 30 and ROM 32. A data bus 38 connects memory 30 and ROM 32 with a data buffer 34 that is further connected to data bus 14D of bus 14. Control lines 40 interconnect BIC 16 and data buffer 34') ('Referring now to the drawings, and first to FIG. 1, there is shown an

exemplary data processing system comprising a personal computer 10 operable under an operating system to execute application programs ') ('Executor 332 then transfers control along one of three different paths dependent upon how it was invoked. For all three paths, the first steps 340, 348, and 352 are to save the contents of the DSP registers by storing the contents thereof in the task control block of the task being interrupted.')

It is noted again that Baker teaches of a method for transmitting functions. As discussed for claim 1, the transfer of functions and records or any other type of data is analogous in the art of multicomputer data transferring, and is thus considered an insignificant difference.

As per claim 11 Baker teaches a real time control system where in the operating system manages the memory so that the internal memory is allocated when the digital signal processor is required to perform fast processing on a task and so that the external memory is allocated when the internal memory is completely allocated (col. 4 lines 5-63, col. 10 line 10-65)) ('BIC 16 performs two primary functions, one being that of a memory controller for accessing a main memory 30 and a ROM 32. Main memory is a dynamic random access memory (RAM) that comprises a plurality of single, in-line, memory modules (SIMMS) and stores application programs 31 for execution by microprocessor 12 and math coprocessor 18. ROM 32 stores a power on self test (POST) program 33. POST program 33 performs the primary test, i.e. POST, of the system when computer 10 is restarted by turning the power on or by a keyboard reset. An address and control bus 36 connects BIC 16 with memory 30 and ROM 32. A data bus 38 connects memory 30 and ROM 32 with a data buffer 34 that is further connected to data bus 14D of bus 14. Control lines 40 interconnect BIC 16 and data buffer 34') ('Referring now to the

drawings, and first to FIG. 1, there is shown an exemplary data processing system comprising a personal computer 10 operable under an operating system to execute application programs ') ('Executor 332 then transfers control along one of three different paths dependent upon how it was invoked. For all three paths, the first steps 340, 348, and 352 are to save the contents of the DSP registers by storing the contents thereof in the task control block of the task being interrupted.')

It is noted again that Baker teaches of a method for transmitting functions. As discussed for claim 1, the transfer of functions and records or any other type of data is analogous in the art of multicomputer data transferring, and is thus considered an insignificant difference.

As per claim 12, Baker teaches a real time control system wherein the operating system manages the memory so that the external memory is divided into a plurality of memories using the memory structure (col. 4 lines 5-63) ('BIC 16 performs two primary functions, one being that of a memory controller for accessing a main memory 30 and a ROM 32. Main memory is a dynamic random access memory (RAM) that comprises a plurality of single, in-line, memory modules (SIMMS) and stores application programs 31 for execution by microprocessor 12 and math coprocessor 18. ROM 32 stores a power on self test (POST) program 33. POST program 33 performs the primary test, i.e. POST, of the system when computer 10 is restarted by turning the power on or by a keyboard reset. An address and control bus 36 connects BIC 16 with memory 30 and ROM 32. A data bus 38 connects memory 30 and ROM 32 with a data buffer

34 that is further connected to data bus 14D of bus 14. Control lines 40 interconnect BIC 16 and data buffer 34')

It is noted again that Baker teaches of a method for transmitting functions. As discussed for claim 1, the transfer of functions and records or any other type of data is analogous in the art of multicomputer data transferring, and is thus considered an insignificant difference.

As per claim 13, Baker teaches a real time control system, wherein the operating system allocates and returns the memory in units of predetermined-sized pages in a system call way, and checks allocation or non-allocation of the memory on the basis of the map of a memory (col. 4 lines 5-63) ('BIC 16 performs two primary functions, one being that of a memory controller for accessing a main memory 30 and a ROM 32. Main memory is a dynamic random access memory (RAM) that comprises a plurality of single, in-line, memory modules (SIMMS) and stores application programs 31 for execution by microprocessor 12 and math coprocessor 18. ROM 32 stores a power on self test (POST) program 33. POST program 33 performs the primary test, i.e. POST, of the system when computer 10 is restarted by turning the power on or by a keyboard reset. An address and control bus 36 connects BIC 16 with memory 30 and ROM 32. A data bus 38 connects memory 30 and ROM 32 with a data buffer 34 that is further connected to data bus 14D of bus 14. Control lines 40 interconnect BIC 16 and data buffer 34') It is noted again that Baker teaches of a method for transmitting functions. As discussed for claim 1, the transfer of functions and records or any other type of data is analogous in the art of multicomputer data transferring, and is thus considered an insignificant difference.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nilesh R Shah whose telephone number is 703-305-8105. The examiner can normally be reached on Monday-Friday 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Grant can be reached on 703-308-1108. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

NS

December 9, 2003